§Department of Electrical & Electronic Engineering

EE2 Circuits and Systems

Module Description and Plan

Peter Cheung, v2.0, 10 Oct. 2021

Introduction

Coronavirus pandemic has forced us to adapt a "mixed-mode" delivery of our teaching during the Autumn term of 2021-2022 session when the 2nd year EEE Circuits and Systems module is delivered with in-person provisions where possible. This document provides a detail plan on how I plan to achieve this without compromising the learning outcomes for this module. The purpose is to inform both students taking, and staff/GTAs assisting with this module to prepare and plan ahead of the Autumn.

This module is new from last year for EEE students after the curriculum reform two years earlier. It covers both the analogue and digital electronics from previous incarnation of our programme. It follows from the Year 1 modules on Analysis and Design of Circuits and Digital Electronics & Computer Architecture.

Aims and Objectives

The goal of the Circuits and Systems module is to prepare you for elective courses in the third and fourth years. In some cases, it might even help some of you with third-year industrial placement in the electronics sector. The emphasis will be on systems view of circuits, the relationship between analogue and digital electronics and the interfacing between the two, the implication of non-ideal behaviour in electronic circuits such as noise and bandwidth limitations, the building blocks for both analogue and digital electronics sub-systems and the method used to design such sub-circuits.

Learning Outcomes

By the end of this module, students will be able to:

- Partition an electronic system into its analogue and digital constituent parts and explain the interaction between the two parts
- Specify suitable interfaces between the two and explain the implications and limitations of such interfaces (e.g. resolution, data communication rate etc.)
- Explain the different methods used to convert between analogue and digital domain and to choose the appropriate one to meet system level specifications
- Analyse and design active analogue filters using operation amplifiers to meet system level specifications in both frequency and time domains
- Specify at system level noise level allowed at different stages of the analogue sub-systems and the engineering practices required to meet such noise requirements
- Describe building blocks in typical digital systems, their functions and how they may be specified in a hardware description language such as Verilog HDL
- Analyse timing constraints in digital circuits and derive maximum operating frequency in a given synchronous circuit
- Design, specify and synthesize synchronous control circuits as Finite State Machines
- Design, simulate and implement medium complexity digital sub-systems using various building blocks such as FSM, counters, memory block and arithmetic circuits
- Use a combination of analogue and digital circuits to process audio electrical signals to achieve specific goals

Implications of Multi-Mode Delivery

This module will be delivered with four separate components:

1. **Lectures & Problem Classes** – There will be two-hours scheduled lectures every week to cover the taught materials, and a one-hour problem class to discuss problem sheets and laboratory work in general. Multi-mode delivery means that these will be delivered to live audiences. Students attending in person must wear face coverings, obey College's COVID guidelines. All such classes will also be streamed live online with MS Teams for those who attend remotely, and recorded for those who want to watch afterwards, either for the first time, or for revision.

2. **Practical Experiment Sessions** – There will be two 2-hours supervised laboratory session every week. Student in a cohort will be divided into pairs sharing a Lab Bench. You may choose your own Lab Partner. If you don't have one, one will be assigned to you. You are also encourage to form teams of four or six students. The idea is that you will work with your partner and the team members to help each other and exchange ideas either remotely or in the lab.

3. Students attending lab sessions in-person will be allocated individual benches, must bring their own laptop and their Lab-in-a-Box, and they must obey the strict social distancing guidelines. They must also wear face coverings during Lab.

   During the scheduled lab session, staff and GTAs will be on hand to offer help and answer questions. They will be wearing face covering.

   Staff/GTA will also be handling any queries remotely via MS Teams on a first-come-first-served basis.

4. **Forum** – We encourage students to help each other as a community of scholars. Therefore, we will use the MS Team's Forum as a platform for students to post questions and issues, and others to contribute towards solutions. Staff will monitor the forum and validate solutions suggested. Those who contribute most to the Forum will be awarded bonus marks (see later) at the module leader's discretion.

Practical Experimentation – Lab-in-a-Box

As with some other modules in the second year, you will be issued, on a loan basis, individual Lab-in-a-Box for you to conduct practical experiments for this module. In this way, you will not need to share your set of lab equipment, boards or components with anyone else, whether you are physically in the Lab or work remotely at home, in London or elsewhere in the world. The Laboratory Kit for this module will include:

- A USB-based dual channel oscilloscope, shared with other modules
- A breadboard with a set of components to build analogue circuits
- A FPGA educational board (the DE10-Lite) to test digital designs on FPGAs
- A proto-shield add-on module for the FPGA board intended for ADC and DAC chips
- Other modules for the Challenges associated with in this module

Assessment

Assessment for this module will consists of three components: 1) a written examination at the end of the year (60%), 2) a mid-term lab oral assessment on Lab 1 to 3 (15%), 3) a final Lab Oral of everything (25%).

There is a further 1 to 5% **bonus marks** awarded at my discretion to a small number of individuals whom the module leader judges to have made exceptional contributions to the Forum.

The Teaching Team

Module Leader:	Prof Peter YK Cheung
Other staff:	Dr Ed Stott, Dr Christos Papavassilou
GTAs:	Benjamin Chua, Sina Boroumand

Preliminary Plan for CAS module (subject to change)

Week	Lectures & Problem Classes	Lab Experiment	Contents and Learning outcomes
2 11 Oct	**Lecture 1**– Introduction to electronic systems & the Circuits and Systems module	**Lab 0** Unpacking Lab-in-a-Box & Set up	Overview of module and links with Year 1 and Year 3; analogue vs digital sub-system in electronics; signal vs noise in electronics.
3 18 Oct	**Lecture 2**[1] – Amplification of electrical signals & operational amplifiers Class 1: Discussion on Lab 1	**Lab 1** Amplication and Op-amps	Amplification of signals; operational amplifier sources of errors; limitations of op-amps; intepretation of datasheets; using op-amp in practical electronics.
4 25 Oct	**Lecture 3**[1] – Anatomy of the LM386 audio amplifier Class 2: Discussion Problem sheet 1 part 1 & Lab 2	**Lab 2** Op-amps Applications	Three stages of LM386; Actual LM386 implementations; linearity in amplifier; driving low impedance load; gain-bandwidth products.
5 1 Nov	**Lecture 4**[1] – Application of Op-Amps Class 3: Problem sheet 1 part 2 & discussions on Lab Oral	**Lab 3** Setting up and using DE10-Lite with Quartus	Rectifier and peak detection circuits; oscillators; square wave and triangular wave generators; analogue comparator with hysteresis (schmitt trigger circuit); analogue PWM; Butterworth filters; Salley-Key filters.
6 8 Nov		Interim Lab Oral (Lab 1 & 2 only)	No new materials this week – only catch up and oral examination.
7 15 Nov	**Lecture 5** – Digital design with FPGAs **Lecture 6** – Verilog HDL Class 5: Problem sheet 2 and discssion on Lab 4	**Lab 4** FSM design	Modern digital technology; full-custom, semi-custom and reconfigurable hardware; FPfGA architecture and evolution; digital design flow; gates, flip-flops/registers, counters, shift registers, multiplexers, decoders/encoders; Verilog as a HDL; basic structure of Verilog; specifying bsic building blocks in Verilog; 7-segment decoders; binary to BCD decoder; specify synchronous circuits in Verilog.
8 22 Nov	**Lecture 7** – FSM design and SPI interface **Lecture 8** – Timing constraints & timing analysis Class 6: Problem sheet 3 and discuss Lab 5	**Lab 5** SPI interface to DAC & Sinewave generation	FSM design flow; designing complex FSM; FSM specification in Verilog.SPI interface protocol; design to meet timing constraints; SPI specification in Verilog explained. Timing specification; timing analysis; timing violations; maximum operating frequency; maximum throughput.
9 29 Nov	**Lecture 9** – D-to-A converters **Lecture 10** – A-to-D converters Class 7: Problem sheet 4 and discuss Lab 6	**Lab 6** Echo sythesizer	how to interprete DAC datasheet; resistor string architecture; R-2R architecture; oversample DAC, PWM DAC; Flash ADC; counting ADC; dual-slope ADC; SAR ADC; DAC/ADC used with DE10 board.
10 6 Dec	**Lecture 11** – Memory organisation, Address decoding **Lecture 12** - Embedded memory and DSP blocks Class 8: Problem sheet 5 and discuss Open-ended challenges	Open-ended challenges	RAM, ROM, Flash memory, DRAM; memory organisation; addressing space; address decoding; Embedded memory block in FPGA; DSP block and its used for filtering; other FPGA blocks not used in this module.
11 13 Dec	**Lecture 13** – System level design considerations Class 9: Open-ended challenges & Lab 6	Final Lab Oral	System busses and bus protocols.System level view of circuits; noise sources and practical methods to control noise in circuits and systems; interfacing and interconnection issues. Main lab oral assessment